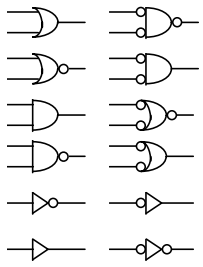
Combinational Logic

Gate Symbols

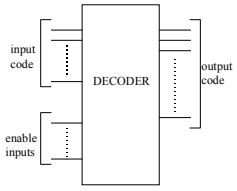
- OR
- NOR
- AND
- NAND
- INVERTER
- BUFFER



- Exercise : show that the equivalent gates do the same function

Decoder

- Multiple-input/multiple-output device.
- Inputs (n) are less than outputs (m).
- Converts input code words into output code words.
- One-to-One mapping :
  - Each input code produces only one output code.



MSI 2-to-4 Decoder

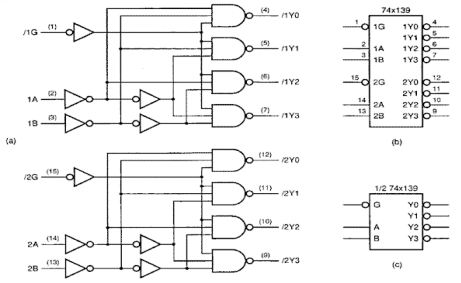


Figure 5–26 The 74x139 dual 2-to-4 decoder: (a) logic diagram, including pin numbers for a standard 16-pin dual in-line package; (b) traditional logic symbol; (c) logic symbol for one decoder.

MSI 3-to-8 Decoder

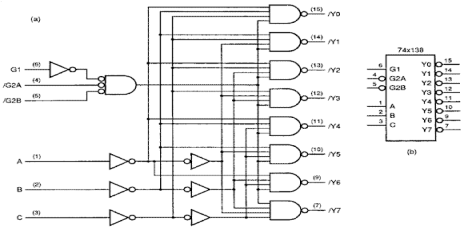
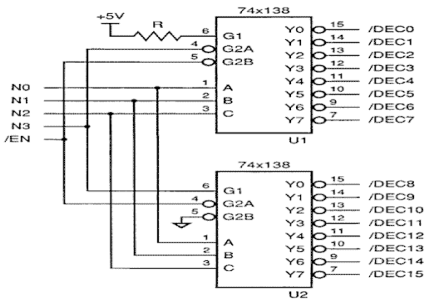
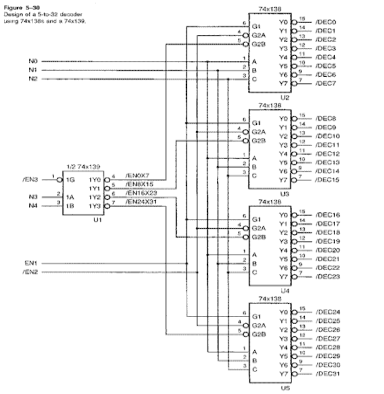


Figure 5–28 The 74x138 3-to-8 decoder: (a) logic diagram, including pin numbers for a standard 16-pin dual in-line package; (b) traditional logic symbol.

Cascading Decoders: 4-to-16 Decoder

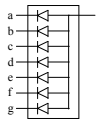


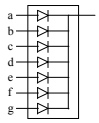
Cascading Decoders:
5-to-32 Decoder

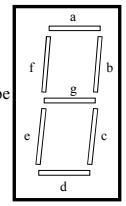


Seven-Segment Displays

- Displays decimal numbers and some characters
- LED (Light Emitting Diode) or
  LCD (Liquid Crystal Display)
- LED type
  - Common Anode(CA) /Common Cathod(CC) type



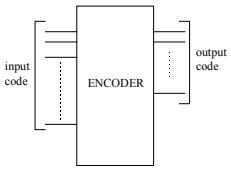




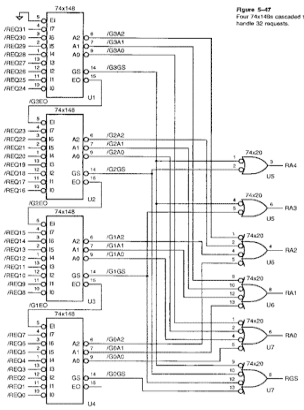
  - CA : requires Active Low inputs (a driver with Active Low outputs)
  - CC : requires Active High inputs (a driver with Active High outputs)

Encoders

- Multiple-input/multiple-output device.
- Perfoms the inverse function of a Decoder.
- Outputs (m) are less than inputs (n).
- Converts input code words into output code words.

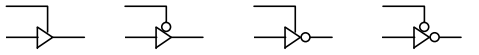


Cascading Encoders : 32-to-5 Encoder



Three State Buffers/Drivers

- A buffer/inverter with enable input



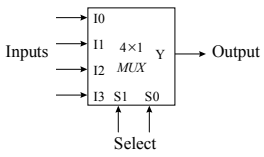
Buffer Actice High Enable | Buffer Actice Low Enable | Inverter Active High Enable | Inverter Actice Low Enable

- The ouput is floating (High Impedance, Hi-Z) when the enable input is deasserted (The input is isolated from the output)
- Application:
  Controlling the access of a single line/bus by multiple devices

Multiplexers

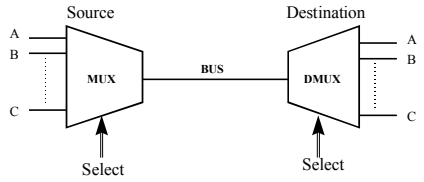
- Multiplexing : transmitting large number of signals over a small number of channels or lines
- Digital multiplexer (MUX) : selects one of many input lines and directs it to a single output.
- Selection lines controls the selection of a particular input
- n selction lines, 2^n inputs , single output.
- Example : 4-to-1 line multiplexer :
  Function Table :

S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3



Demultiplexers

- Demultiplexer (DMUX) performs the opposite function of a MUX.
- A digital Demultiplexer receives input data on a single input and transmits it on one of 2^n possible outputs according to the value of the n select inputs
- MUX/DMUX are used in data transmission



MSI DEMUX : 74x155

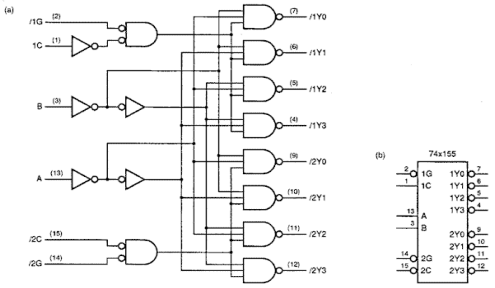
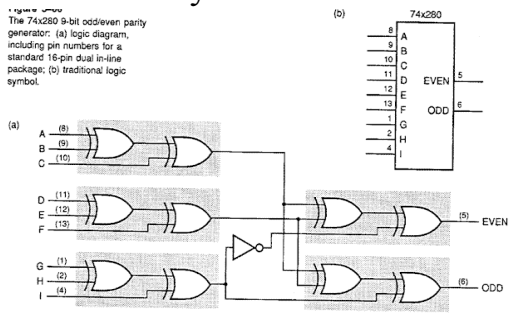


Figure 5–57 The 74x155 2-bit, 4-output demultiplexer: (a) logic diagram, including pin numbers for a standard 16-pin dual in-line package; (b) traditional logic symbol.

MSI Parity Circuit : 74x280

The 74x280 9-bit odd/even parity generator: (a) logic diagram, including pin numbers for a standard 16-pin dual in-line package; (b) traditional logic symbol.



Parity-Checking Application

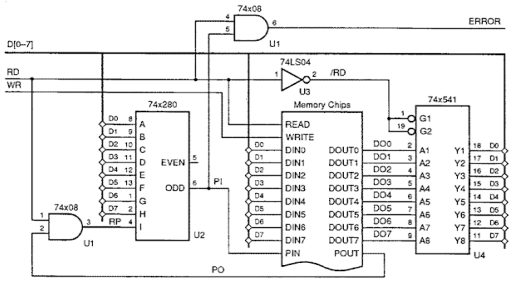
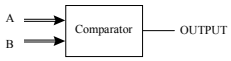


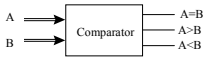
Figure 5–67 Parity generation and checking for an 8-bit-wide memory system.

Comparators

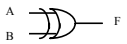
- Compares Two binary words and indicate if they are equal



- Advanced Comparators :



- 1-bit Comparator : XOR gate , the Output is 1 if A<>B



Group-Ripple Adder

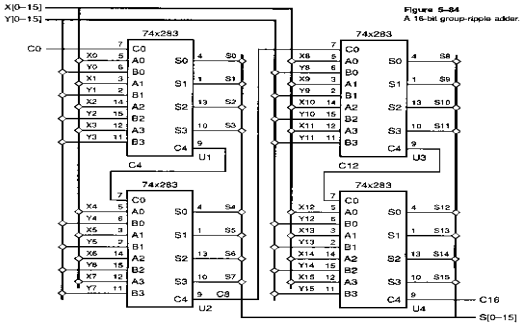


Figure 5–84
A 16-bit group-ripple adder.