

Combinational Logic

Gate Symbols

- OR  
 - NOR  
 - AND  
 - NAND  
 - INVERTER  
 - BUFFER  
- Exercise : show that the equivalent gates do the same function

Decoder

- Multiple-input/multiple-output device.
- Inputs (n) are less than outputs (m).
- Converts input code words into output code words.
- One-to-One mapping :
 - Each input code produces only one output code.

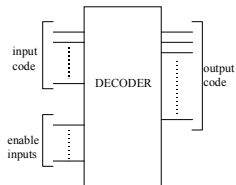


Figure 1 consists of three logic diagrams labeled (a), (b), and (c).
 Diagram (a) shows a 74x139 3-to-8 decoder with inputs 1Q, 1A, and 1B. Its outputs 1Y0, 1Y1, 1Y2, and 1Y3 are connected to four 3-input AND gates. The AND gates are labeled (4), (5), (6), and (7). The outputs of these AND gates are labeled /Y0, /Y1, /Y2, and /Y3. The inputs to the AND gates are combinations of the decoder outputs and their complements.
 Diagram (b) shows a 74x139 3-to-8 decoder with inputs 2G, 2A, and 2B. Its outputs 2Y0, 2Y1, 2Y2, and 2Y3 are connected to four 3-input AND gates. The AND gates are labeled (11), (12), (13), and (14). The outputs of these AND gates are labeled /Y0, /Y1, /Y2, and /Y3. The inputs to the AND gates are combinations of the decoder outputs and their complements.
 Diagram (c) shows a 74x138 3-to-8 decoder with inputs G, A, and B. Its outputs Y0, Y1, Y2, and Y3 are connected to three 3-input AND gates. The AND gates are labeled (1), (2), and (3). The outputs of these AND gates are labeled Y0, Y1, Y2, and Y3. The inputs to the AND gates are combinations of the decoder outputs and their complements.

Figure 1(a) is a logic diagram of the proposed 7-to-138 decoder. It features seven inputs: G_1 , $/Q2A$, $/Q2B$, A , B , C , and $/Q2C$. The outputs are labeled Y_0 through Y_{17} . The circuit includes a 74x138 decoder and a 74x139 decoder. The 74x138 decoder has inputs G_1 , $/Q2A$, and $/Q2B$, and outputs Y_0 through Y_7 . The 74x139 decoder has inputs A , B , and C , and outputs Y_{10} through Y_{17} . The 74x138 decoder is connected to the 74x139 decoder via its $/Q2C$ output and its $/Q2A$ and $/Q2B$ inputs. The 74x139 decoder is connected to the 74x138 decoder via its G_1 input and its $/Q2A$ and $/Q2B$ inputs. The 74x138 decoder is connected to the 74x139 decoder via its $/Q2C$ output and its $/Q2A$ and $/Q2B$ inputs. The 74x139 decoder is connected to the 74x138 decoder via its G_1 input and its $/Q2A$ and $/Q2B$ inputs.

Figure 1(b) shows the pinout of the 74x138 decoder. It is a 16-pin package with the following connections:

Pin	Signal
6	G_1
1	$/Q2A$
3	$/Q2B$
15	Y_0
14	Y_1
13	Y_2
12	Y_3
11	Y_4
10	Y_5
9	Y_6
8	Y_7

The diagram illustrates a 74x138 decoder circuit for a 32-bit address bus. It consists of two 74x138 decoders, U1 and U2. The inputs to U1 are G1 (connected to +5V), G2A (connected to R), and G2B (connected to 5). The outputs of U1 are Y0 through Y7, labeled /DEC0 through /DEC7. The inputs to U2 are G1 (connected to 6), G2A (connected to 4), and G2B (connected to 5). The outputs of U2 are Y0 through Y7, labeled /DEC8 through /DEC15. Address lines N0, N1, N2, and N3 are connected to the inputs of both decoders: N0 to G1 of both, N1 to G2A of both, N2 to G2B of both, and N3 to /EN of both.

Figure 5-38
Design of a 5-to-32 decoder
using 74x138s and a 74x139

Cascading Decoders:
5-to-32 Decoder

Seven-Segment Displays

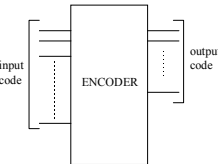
- Displays decimal numbers and some characters
- LED (Light Emitting Diode) or LCD (Liquid Crystal Display)
- LED type
 - Common Anode(CA) /Common Cathod(CC) type

The diagram illustrates the internal structure of a seven-segment display. On the right, a rectangular frame represents the display, with segments labeled 'a' through 'g'. Segment 'a' is the top horizontal bar, 'b' is the top-right vertical bar, 'c' is the bottom-right vertical bar, 'd' is the bottom horizontal bar, 'e' is the bottom-left vertical bar, 'f' is the top-left vertical bar, and 'g' is the middle horizontal bar. To the left of this frame, two circuit diagrams show the internal LED connections. The first diagram, labeled 'Common Anode(CA)', shows seven LEDs with their anodes connected to a single common point on the right and their cathodes connected to segments 'a' through 'g' on the left. The second diagram, labeled 'Common Cathode(CC)', shows seven LEDs with their cathodes connected to a single common point on the right and their anodes connected to segments 'a' through 'g' on the left.

- CA : requires Active Low inputs (a driver with Active Low outputs)
- CC : requires Active High inputs (a driver with Active High outputs)

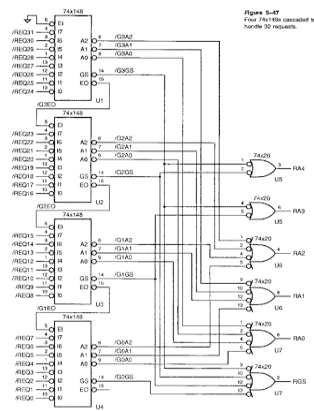
Encoders

- Multiple-input/multiple-output device.
- Performs the inverse function of a Decoder.
- Outputs (m) are less than inputs (n).
- Converts input code words into output code words.



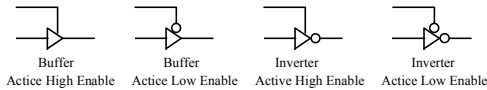
The diagram shows a central rectangular block labeled "ENCODER". To the left of the block, there is a bracket labeled "input code" which groups four horizontal lines entering the block. Inside this group, there are three solid lines at the top and a dashed line below them, indicating a total of four inputs. To the right of the block, there is a bracket labeled "output code" which groups four horizontal lines exiting the block. Inside this group, there are three solid lines at the top and a dashed line below them, indicating a total of four outputs.

Cascading Encoders : 32-to-5 Encoder



Three State Buffers/Drivers

- A buffer/inverter with enable input



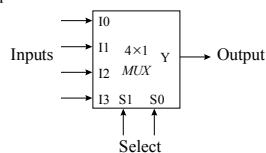
- The output is floating (High Impedance, Hi-Z) when the enable input is deasserted (The input is isolated from the output)
- Application:
Controlling the access of a single line/bus by multiple devices

Multiplexers

- Multiplexing : transmitting large number of signals over a small number of channels or lines
- Digital multiplexer (MUX) : selects one of many input lines and directs it to a single output.
- Selection lines controls the selection of a particular input
- n selection lines, 2^n inputs , single output.
- Example : 4-to-1 line multiplexer :

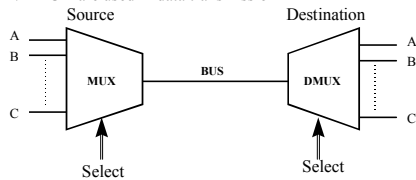
Function Table :

S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3



Demultiplexers

- Demultiplexer (DMUX) performs the opposite function of a MUX.
- A digital Demultiplexer receives input data on a single input and transmits it on one of 2^n possible outputs according to the value of the n select inputs
- MUX/DMUX are used in data transmission



MSI DEMUX : 74x155

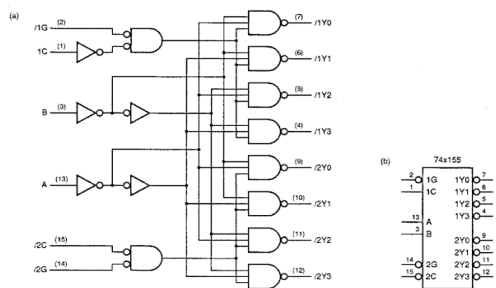
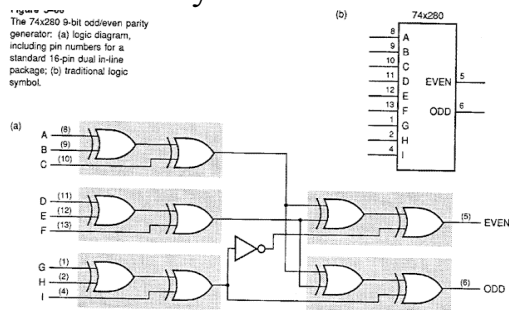


Figure 5-57 The 74x155 2-bit, 4-output demultiplexer: (a) logic diagram, including pin numbers for a standard 16-pin dual in-line package; (b) traditional logic symbol.

MSI Parity Circuit : 74x280

The 74x280 9-bit odd/even parity generator: (a) logic diagram, including pin numbers for a standard 16-pin dual in-line package; (b) traditional logic symbol.



Parity-Checking Application

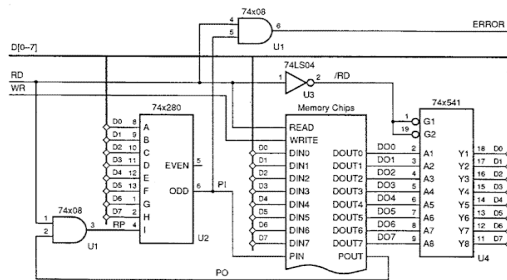
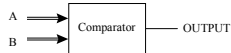


Figure 5-67 Parity generation and checking for an 8-bit-wide memory system.

Comparators

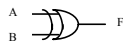
- Compares Two binary words and indicate if they are equal



- Advanced Comparators :



- 1-bit Comparator : XOR gate , the Output is 1 if $A \neq B$



Group-Ripple Adder

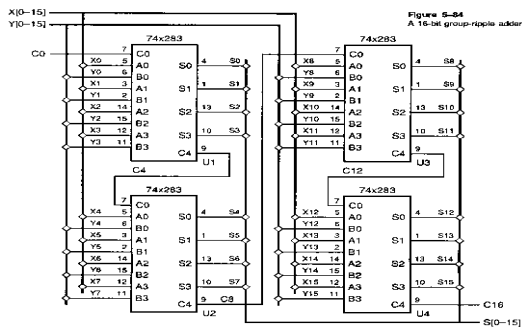


Figure 5-84
A 16-bit group-ripple adder.