Micro Processor & Controller

TMS320F28335 – Concerto
Data Manual

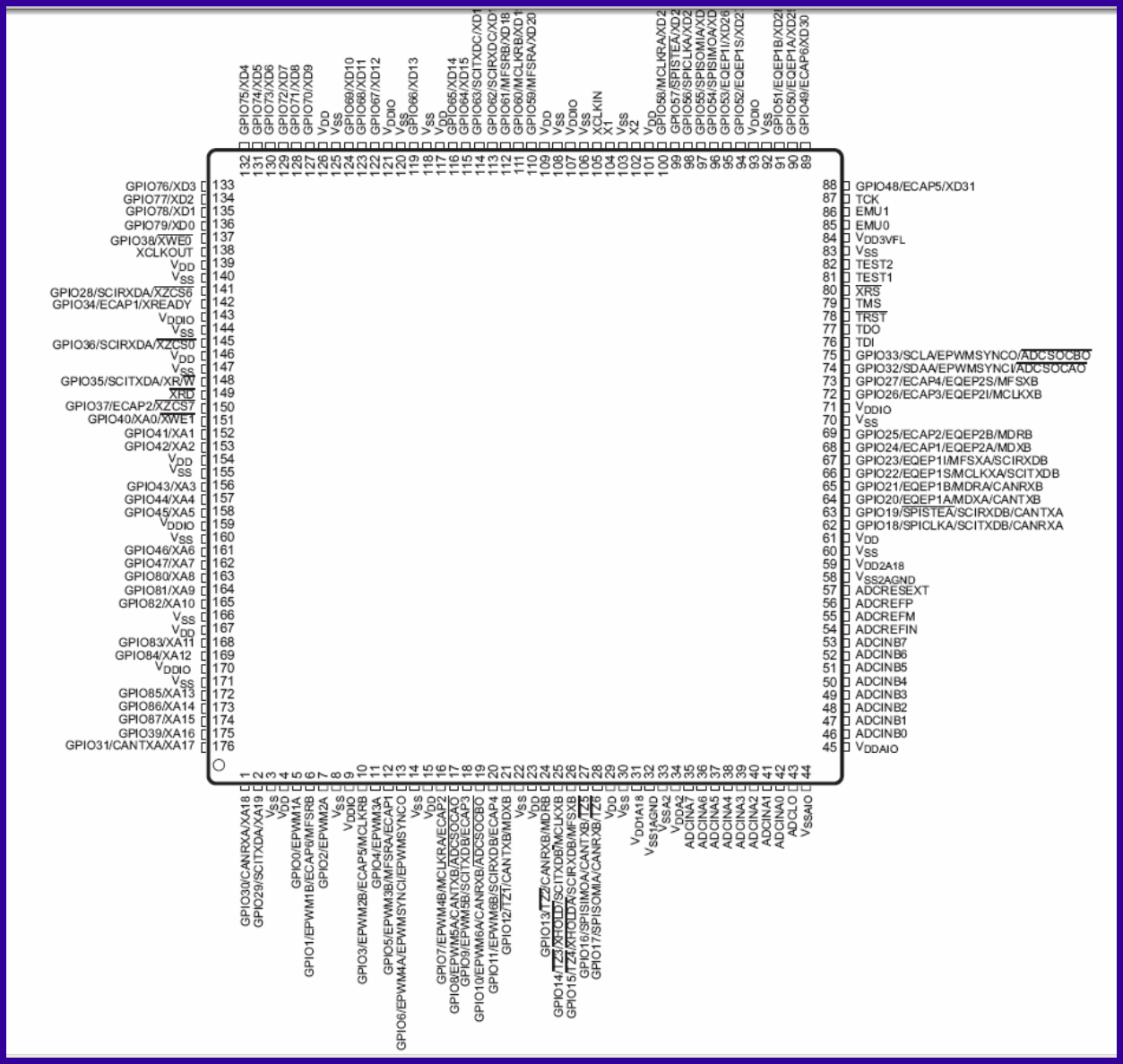
Features

1.1 Features

- High-Performance Static CMOS Technology
  - Up to 150 MHz (6.67-ns Cycle Time)
  - 1.9-V/1.8-V Core, 3.3-V I/O Design
- High-Performance 32-Bit CPU (TMS320C28x)
  - IEEE-754 Single-Precision Floating-Point Unit (FPU) (F2833x only)
  - 16 x 16 and 32 x 32 MAC Operations
  - 16 x 16 Dual MAC
  - Harvard Bus Architecture
  - Fast Interrupt Response and Processing
  - Unified Memory Programming Model
  - Code-Efficient (in C/C++ and Assembly)
- Six Channel DMA Controller (for ADC, McBSP, ePWM, XINTF, and SARAM)
- 16-bit or 32-bit External Interface (XINTF)
  - Over 2M x 16 Address Reach
- On-Chip Memory
  - F28335/F28235: 256K x 16 Flash, 34K x 16 SARAM
  - F28334/F28234: 128K x 16 Flash, 34K x 16 SARAM
  - F28332/F28232: 64K x 16 Flash, 26K x 16 SARAM
  - 1K x 16 OTP ROM
- Boot ROM (8K x 16)
  - With Software Boot Modes (via SCI, SPI, CAN, I2C, McBSP, XINTF, and Parallel I/O)
  - Standard Math Tables
- Clock and System Control
  - Dynamic PLL Ratio Changes Supported
  - On-Chip Oscillator
  - Watchdog Timer Module
- GPIO0 to GPIO63 Pins Can Be Connected to One of the Eight External Core Interrupts
- Peripheral Interrupt Expansion (PIE) Block That Supports All 58 Peripheral Interrupts
- 128-Bit Security Key/Lock
  - Protects Flash/OTP/RAM Blocks
  - Prevents Firmware Reverse Engineering
- Enhanced Control Peripherals
  - Up to 18 PWM Outputs
  - Up to 6 HRPWM Outputs With 150 ps MEP Resolution
  - Up to 6 Event Capture Inputs
  - Up to 2 Quadrature Encoder Interfaces
  - Up to 8 32-bit/Nine 16-bit Timers
- Three 32-Bit CPU Timers
- Serial Port Peripherals
  - Up to 2 CAN Modules
  - Up to 3 SCI (UART) Modules
  - Up to 2 McBSP Modules (Configurable as SPI)
  - One SPI Module
  - One Inter-Integrated-Circuit (I2C) Bus
- 12-Bit ADC, 16 Channels
  - 80-ns Conversion Rate
  - 2 x 8 Channel Input Multiplexer
  - Two Sample-and-Hold
  - Single/Simultaneous Conversions
  - Internal or External Reference
- Up to 88 Individually Programmable, Multiplexed GPIO Pins With Input Filtering
- JTAG Boundary Scan Support (1)
- Advanced Emulation Features
  - Analysis and Breakpoint Functions
  - Real-Time Debug via Hardware
- Development Support Includes
  - ANSI C/C++ Compiler/Assembler/Linker
  - Code Composer Studio™ IDE
  - DSP/BIOS™
  - Digital Motor Control and Digital Power Software Libraries
- Low-Power Modes and Power Savings
  - IDLE, STANDBY, HALT Modes Supported
  - Disable Individual Peripheral Clocks
- Package Options
  - Lead-free Green Packaging
  - Thin Quad Flatpack (PGF)
  - MicroStar BGA™ (ZHH)
  - Plastic BGA (ZJZ)
- Temperature Options:
  - A: –40°C to 85°C (PGF, ZHH, ZJZ)
  - S: –40°C to 125°C (ZJZ)
  - Q: –40°C to 125°C (ZJZ)

(1) IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture

Pin Assignment – 176 LQFP



Pin Descriptions

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2.2 Signal Descriptions

Table 2-3 describes the signals. The GPIO function (shown in Italics) is the default at reset. The peripheral signals that are listed under them are alternate functions. Some peripheral functions may not be available in all devices. See Table 2-1 for details. Inputs are not 5-V tolerant. All pins capable of producing an XINTF output function have a drive strength of 8 mA (typical). This is true even if the pin is not configured for XINTF functionality. All other pins have a drive strength of 4-mA drive typical (unless otherwise indicated). All GPIO pins are I/O/Z and have an internal pullup, which can be selectively enabled/disabled on a per-pin basis. This feature only applies to the GPIO pins. The pullups on GPIO0-GPIO11 pins are not enabled at reset. The pullups on GPIO12-GPIO34 are enabled upon reset.

Table 2-3. Signal Descriptions

NAME	PIN NO.			DESCRIPTION (1)
	PGF PIN #	ZHH BALL #	ZJZ BALL #	
JTAG				
$\overline{TRST}$	78	M10	L11	JTAG test reset with internal pulldown. $\overline{TRST}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: $\overline{TRST}$ is an active high test pin and must be maintained low at all times during normal device operation. An external pulldown resistor is recommended on this pin. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-kΩ resistor generally offers adequate protection. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application. (I, ↓)
TCK	87	N12	M14	JTAG test clock with internal pullup (I, ↑)
TMS	79	P10	M12	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. (I, ↑)
TDI	76	M9	N12	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. (I, ↑)
TDO	77	K9	N13	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. (O/Z 8 mA drive)
EMU0	85	L11	N7	Emulator pin 0. When $\overline{TRST}$ is driven high, this pin is used as an interrupt to or from the emulator system and is defined as input/output through the JTAG scan. This pin is also used to put the device into boundary-scan mode. With the $\overline{EMU0}$ pin at a logic-high state and the EMU1 pin at a logic-low state, a rising edge on the $\overline{TRST}$ pin would latch the device into boundary-scan mode. (IO/Z, 8 mA drive ↑) **NOTE:** An external pullup resistor is recommended on this pin. The value of this resistor should be based on the drive strength of the debugger pods applicable to the design. A 2.2-kΩ to 4.7-kΩ resistor is generally adequate. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application.
EMU1	86	P12	P8	Emulator pin 1. When $\overline{TRST}$ is driven high, this pin is used as an interrupt to or from the emulator system and is defined as input/output through the JTAG scan. This pin is also used to put the device into boundary-scan mode. With the $\overline{EMU0}$ pin at a logic-high state and the EMU1 pin at a logic-low state, a rising edge on the $\overline{TRST}$ pin would latch the device into boundary-scan mode. (IO/Z, 8 mA drive ↑) **NOTE:** An external pullup resistor is recommended on this pin. The value of this resistor should be based on the drive strength of the debugger pods applicable to the design. A 2.2-kΩ to 4.7-kΩ resistor is generally adequate. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application.
FLASH				
V_{DD3VFL}	84	M11	L9	3.3-V Flash Core Power Pin. This pin should be connected to 3.3 V at all times.
TEST1	81	K10	M7	Test Pin. Reserved for TI. Must be left unconnected. (I/O)
TEST2	82	P11	L7	Test Pin. Reserved for TI. Must be left unconnected. (I/O)

(1) I = Input, O = Output, Z = High Impedance, OD = Open drain, ↑ = Pullup, ↓ = Pulldown

Block Diagram

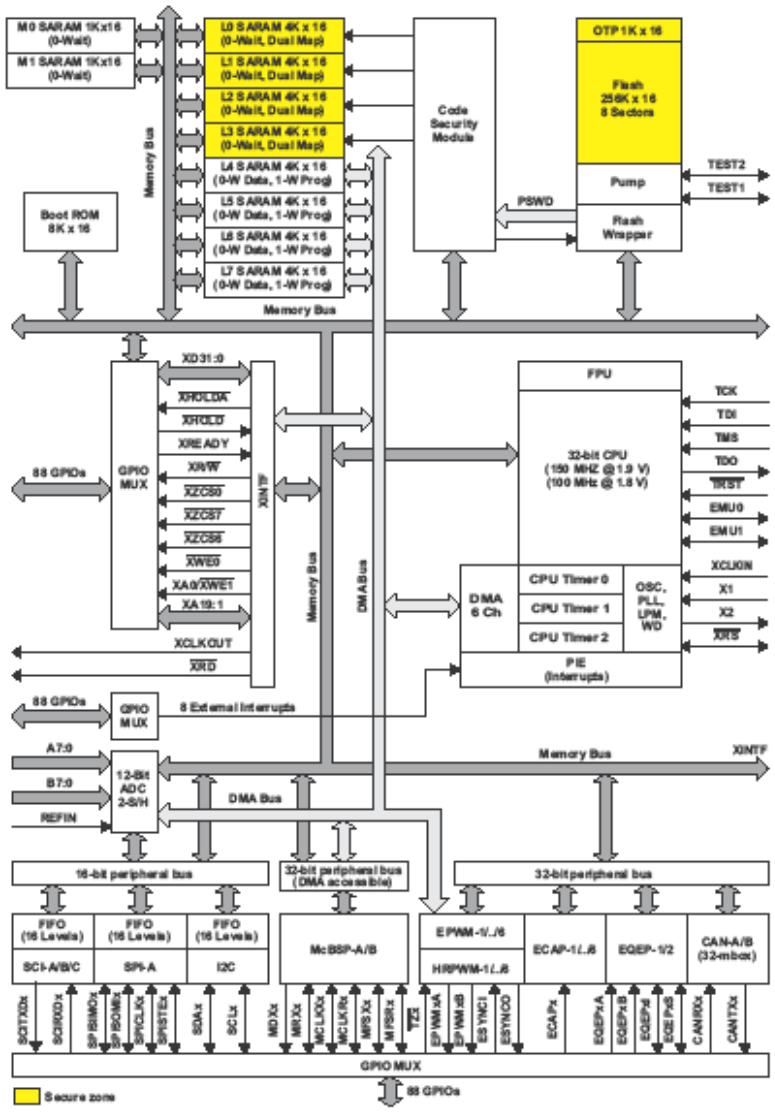
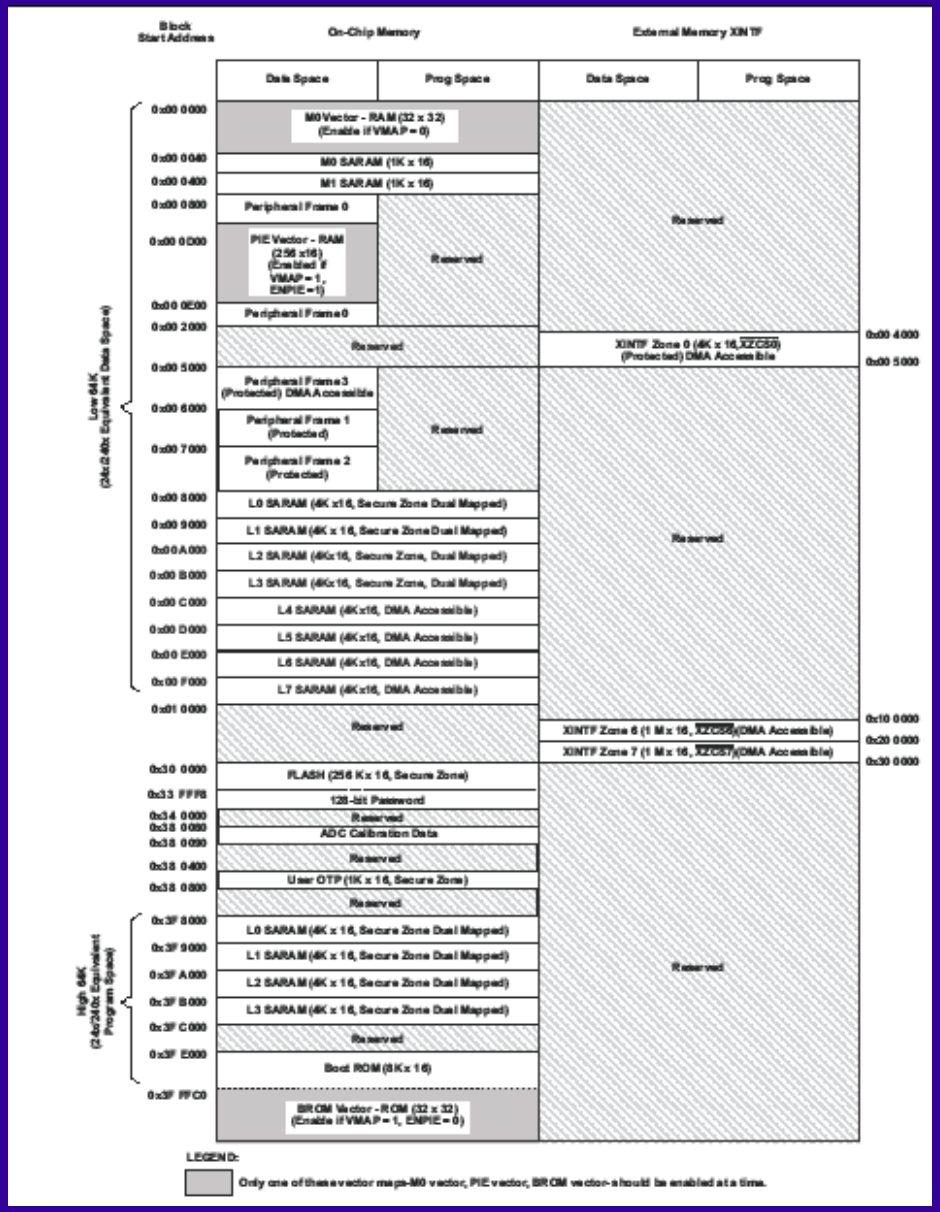


Figure 3-1. Functional Block Diagram

Memory Map


Block Start Address
On-Chip Memory
External Memory XINTF
Data Space
Prog Space
Data Space
Prog Space
0x00 0000
M0 Vector - RAM (32 x 32) (Enable if VMAP = 0)
0x00 0040
M0 SARAM (1K x 16)
0x00 0400
M1 SARAM (1K x 16)
0x00 0800
Peripheral Frame 0
0x00 0D00
PIE Vector - RAM (256 x16) (Enabled if VMAP = 1, ENPIE = 1)
0x00 0E00
Peripheral Frame 0
Reserved
Reserved
0x00 2000
Reserved
0x00 4000
XINTF Zone 0 (4K x 16, XZCS0) (Protected) DMA Accessible
0x00 5000
0x00 5000
Peripheral Frame 3 (Protected) DMA Accessible
0x00 6000
Peripheral Frame 1 (Protected)
0x00 7000
Peripheral Frame 2 (Protected)
Reserved
Reserved
0x00 8000
L0 SARAM (4K x16, Secure Zone Dual Mapped)
0x00 9000
L1 SARAM (4K x 16, Secure Zone Dual Mapped)
0x00 A000
L2 SARAM (4Kx16, Secure Zone, Dual Mapped)
0x00 B000
L3 SARAM (4Kx16, Secure Zone, Dual Mapped)
0x00 C000
L4 SARAM (4Kx16, DMA Accessible)
0x00 D000
L5 SARAM (4Kx16, DMA Accessible)
0x00 E000
L6 SARAM (4Kx16, DMA Accessible)
0x00 F000
L7 SARAM (4Kx16, DMA Accessible)
Low 64K (24x240x Equivalent Data Space)
0x01 0000
Reserved
0x10 0000
XINTF Zone 6 (1 M x 16, XZCS6) (DMA Accessible)
0x20 0000
XINTF Zone 7 (1 M x 16, XZCS7) (DMA Accessible)
0x30 0000
0x30 0000
FLASH (256 K x 16, Secure Zone)
0x33 FFF8
128-bit Password
0x34 0000
Reserved
0x38 0000
ADC Calibration Data
0x38 0090
Reserved
0x38 0400
User OTP (1K x 16, Secure Zone)
0x38 0800
Reserved
Reserved
0x3F 8000
L0 SARAM (4K x 16, Secure Zone Dual Mapped)
0x3F 9000
L1 SARAM (4K x 16, Secure Zone Dual Mapped)
0x3F A000
L2 SARAM (4K x 16, Secure Zone Dual Mapped)
0x3F B000
L3 SARAM (4K x 16, Secure Zone Dual Mapped)
0x3F C000
Reserved
0x3F E000
Boot ROM (8K x 16)
0x3F FFC0
BROM Vector - ROM (32 x 32) (Enable if VMAP = 1, ENPIE = 0)
High 64K (24x240x Equivalent Program Space)
LEGEND:
Only one of these vector maps-M0 vector, PIE vector, BROM vector-should be enabled at a time.

CPU

3.2.1 C28x CPU

The F2833x/F2823x (C28x+FPU) family is a member of the TMS320C2000™ digital signal controller (DSC) platform. The C28x+FPU based controllers have the same 32-bit fixed-point architecture as TI's existing C28x DSCs, but also include a single-precision (32-bit) IEEE 754 floating-point unit (FPU). It is a very efficient C/C++ engine, enabling users to develop their system control software in a high-level language. It also enables math algorithms to be developed using C/C++. The device is as efficient in DSP math tasks as it is in system control tasks that typically are handled by microcontroller devices. This efficiency removes the need for a second processor in many systems. The 32 x 32-bit MAC 64-bit processing capabilities enable the controller to handle higher numerical resolution problems efficiently. Add to this the fast interrupt response with automatic context save of critical registers, resulting in a device that is capable of servicing many asynchronous events with minimal latency. The device has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables it to execute at high speeds without resorting to expensive high-speed memories. Special branch-look-ahead hardware minimizes the latency for conditional discontinuities. Special store conditional operations further improve performance.

The F2823x family is also a member of the TMS320C2000™ digital signal controller (DSC) platform but it does not include a floating-point unit (FPU).

Memory Bus

3.2.2 *Memory Bus (Harvard Bus Architecture)*

As with many DSC type devices, multiple busses are used to move data between the memories and peripherals and the CPU. The C28x memory bus architecture contains a program read bus, data read bus and data write bus. The program read bus consists of 22 address lines and 32 data lines. The data read and write busses consist of 32 address lines and 32 data lines each. The 32-bit-wide data busses enable single cycle 32-bit operations. The multiple bus architecture, commonly termed Harvard Bus, enables the C28x to fetch an instruction, read a data value and write a data value in a single cycle. All peripherals and memories attached to the memory bus will prioritize memory accesses. Generally, the priority of memory bus accesses can be summarized as follows:

Highest:	Data Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Program Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Data Reads	
	Program Reads	(Simultaneous program reads and fetches cannot occur on the memory bus.)
Lowest:	Fetches	(Simultaneous program reads and fetches cannot occur on the memory bus.)