Chapter 1

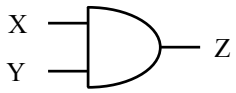
Combinational Logic

Process Control

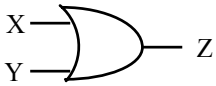
Chapter Outline

- Documentation Standards for digital systems.
- Combinational Logic Design Structures :
  - Logic Gates
  - Decoders
  - Encoders
  - Three-State Buffers
  - Multiplexers
  - Demultiplexers
  - Adders

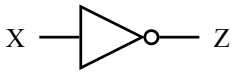
Basic logic Gates



AND



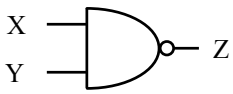
OR



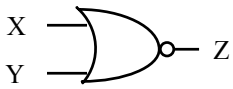
NOT

X	Y	Z		X	Y	Z		X	Z
0	0	0		0	0	0		0	1
0	1	0		0	1	1		1	0
1	0	0		1	0	1			
1	1	1		1	1	1			

No Basic logic Gates



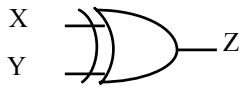
NAND



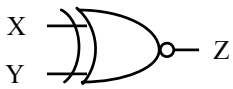
NOR

X	Y	Z				X	Y	Z
0	0	1				0	0	1
0	1	1				0	1	0
1	0	1				1	0	0
1	1	0				1	1	0

No Basic logic Gates



XOR



NXOR

X	Y	Z				X	Y	Z
0	0	0				0	0	1
0	1	1				0	1	0
1	0	1				1	0	0
1	1	0				1	1	1

Timing Diagrams

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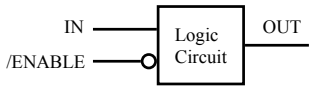
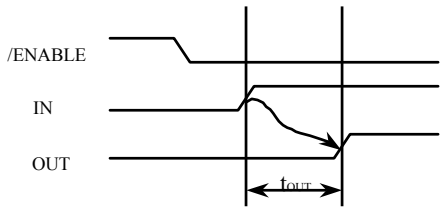
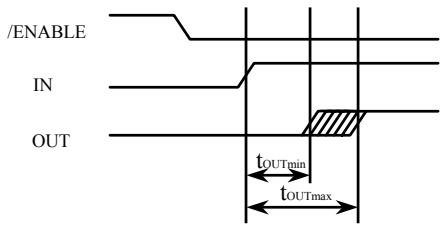
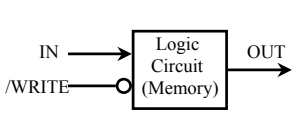


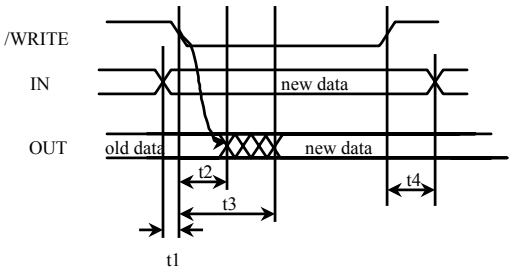


- Delay depends on
  - Internal circuit structure
  - Logic Family type
  - Source Voltage
  - Temperature



Timing Diagram for Data signals (Bus)

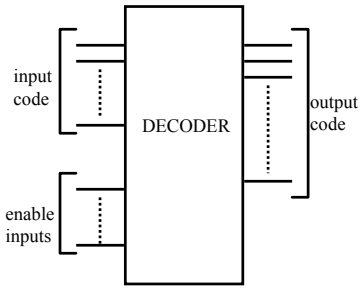




- t1 : t setup
- t2 : t OUTmin
- t3 : t OUTmax
- t4 : t hold

Decoder

- Multiple-input/multiple-output device.
- Inputs (n) are less than outputs (m).
- Converts input code words into output code words.
- One-to-One mapping :
  - Each input code produces only one output code.
- Input codes :
  - Binary Code
  - Gray Code
  - BCD Code
  - Your Code !



Binary Decoder

- n-to-2^n decoder : n inputs and 2^n outputs.
- Input code : Binary Code.
- Output code : 1-out-of-2^n , One output is asserted for each input code.
- Example : n=2, 2-to-4 decoder
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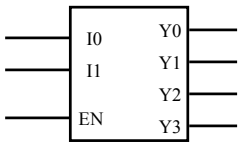
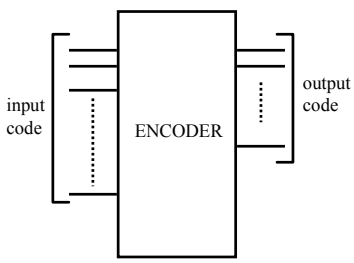
Inputs			Outputs			
EN	I_1	I_0	Y_3	Y_2	Y_1	Y_0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0



Encoders

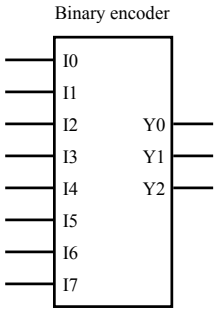
- Multiple-input/multiple-output device.
- Perfoms the inverse function of a Decoder.
- Outputs (m) are less than inputs (n).
- Converts input code words into output code words.



Binary Encoder

- 2^n-to-n encoder : 2^n inputs and n outputs.
- Input code : 1-out-of-2^n.
- Output code : Binary Code
- Example : n=3, 8-to-3 encoder

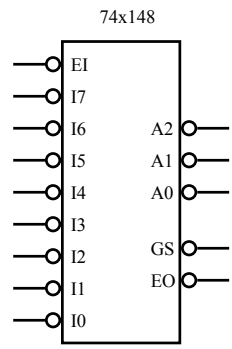
Inputs								Outputs		
I0	I1	I2	I3	I4	I5	I6	I7	Y0	Y1	Y2
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1



Priority Encoder

- 74x148

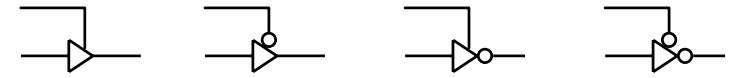
Inputs									Outputs				
/EI	/I0	/I1	/I2	/I3	/I4	/I5	/I6	/I7	/A2	/A1	/A0	/GS	/EO
1	x	x	x	x	x	x	x	x	1	1	1	1	1
0	x	x	x	x	x	x	x	0	0	0	0	0	1
0	x	x	x	x	x	x	0	1	0	0	1	0	1
0	x	x	x	x	x	0	1	1	0	1	0	0	1
0	x	x	x	x	0	1	1	1	0	1	1	0	1
0	x	x	x	0	1	1	1	1	1	0	0	0	1
0	x	x	0	1	1	1	1	1	1	0	1	0	1
0	x	0	1	1	1	1	1	1	1	1	0	0	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0



- /GS is asserted if any of the inputs is selected
- /EO is asserted when no input is selected (used for cascading encoders)

Three State Buffers/Drivers

- A buffer/inverter with enable input



Buffer Actice High Enable | Buffer Actice Low Enable | Inverter Active High Enable | Inverter Actice Low Enable

- The ouput is floating (High Impedance, Hi-Z) when the enable input is deasserted (The input is isolated from the output)
- Application:
  Controlling the access of a single line/bus by multiple devices

Multiplexers

- Multiplexing : transmitting large number of signals over a small number of channels or lines
- Digital multiplexer (MUX) : selects one of many input lines and directs it to a single output.
- Selection lines controls the selection of a particular input
- n selction lines, 2^n inputs , single output.
- Example : 4-to-1 line multiplexer :
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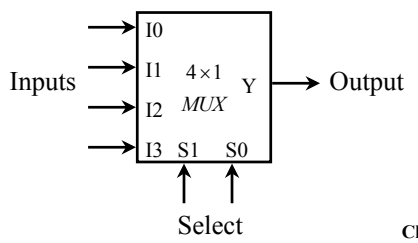
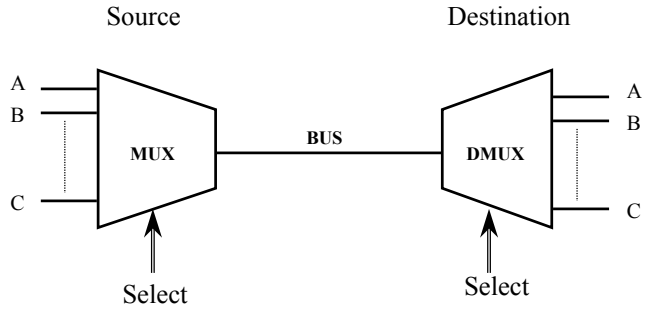
Function Table :

S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3



Demultiplexers

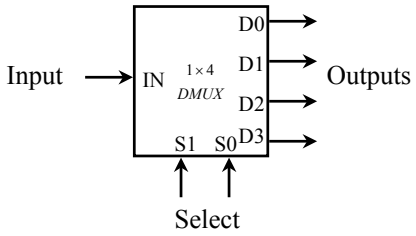
- Demultiplexer (DMUX) performs the opposite function of a MUX.
- A digital Demultiplexer receives input data on a single input and transmits it on one of 2^n possible outputs according to the value of the n select inputs
- MUX/DMUX are used in data transmission



1-to-4 DMUX

- 1-to-4 DEMUX Function Table

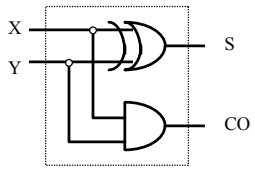
IN	S1	S0	D0	D1	D2	D3
x	0	0	IN	0	0	0
x	0	1	0	IN	0	0
x	1	0	0	0	IN	0
x	1	1	0	0	0	IN



Half Adder

- Truth table :

X	Y	S=(X+Y)	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



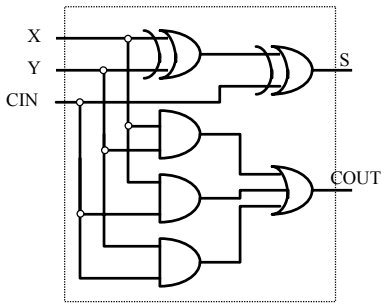
- $S = X \oplus Y$

  $CO = X \bullet Y$

Full Adder

- Truth Table

X	Y	CIN	S	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



- S = X'Y'CIN+ X'YCIN'+XY'CIN'+XYCIN
  $S = X \oplus Y \oplus CIN$
- COUT=XY+X CIN+Y CIN