Chapter 2

Sequential Logic Design

Process Control

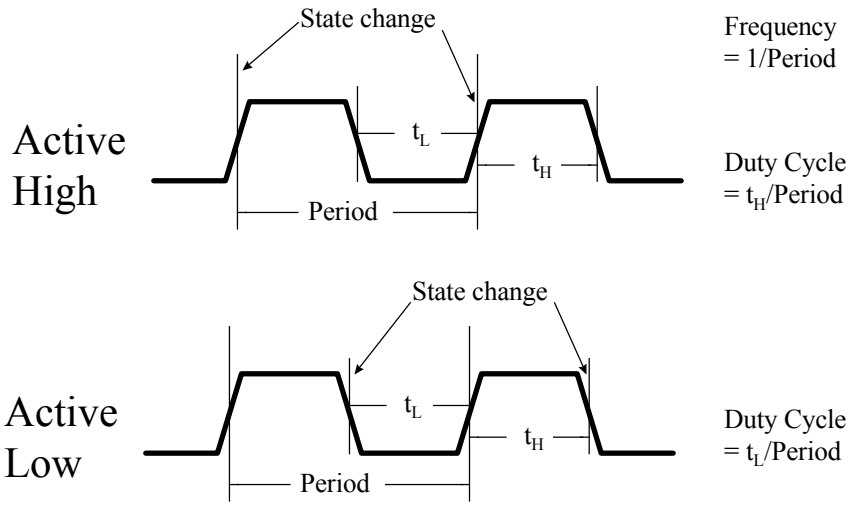
Logic Devices

- Logic devices divide into two major types:
- **Combinational Logic**
  - Current output depends on current input only
  - Gates, decoders, multiplexers, ALUs
- **Sequential Logic**
  - Current output depends on past inputs as well as current input
  - Thus has a memory (usually called the state)
  - Latches, flip-flops, state machines, counters, shift registers

Sequential Logic Definitions

- **Clock** - the master timing element behind the state changes of most sequential circuits.
  - a clock signal is active high if the state changes occur at the rising edge
  - and active low if state changes occur at the falling edge.
- **Clock Period** - time between successive transitions in the same direction.
- **Clock Frequency** - reciprocal of the clock period.
- **Duty Cycle** - the percentage of time that a clock is at its assertion level.

Clock Characteristics



What Are Latches and Flip-flops?

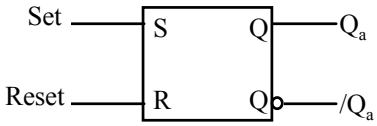
- Common feedback sequential circuits
- Latch
  - Single-bit storage (memory)
  - Changes state at any time due to input change
- Flip-flop
  - Also single-bit storage
  - Changes state ONLY when a clock edge or pulse is applied

Types of Latches and Flip-flops

- Latches
  - S-R Latch
  - S-R Latch with Enable
  - D Latch
- Flip-flops
  - Edge-Triggered D Flip-Flop
  - Edge-Triggered S-R Flip-Flop
  - Edge-Triggered J-K Flip-Flop
  - T Flip-Flop

S-R Latch

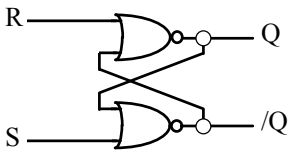
Symbol



Function Table

	S	R	Q	/Q
Hold	0	0	Last Q	Last /Q
Reset	0	1	0	1
Set	1	0	1	0
ILLEGAL	1	1	0	0

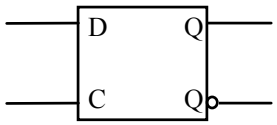
Schematic

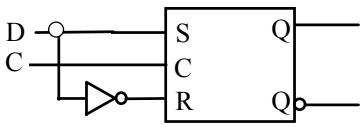


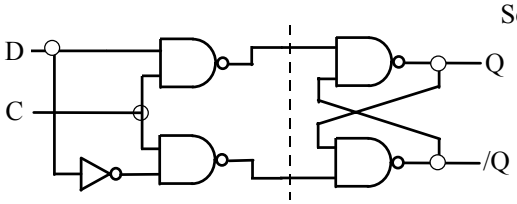
Consider:

- Timing Diagram
- Propagation delay
- Minimum pulse width
- Oscillation

D Flip-Flop



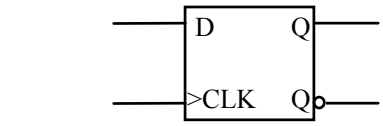




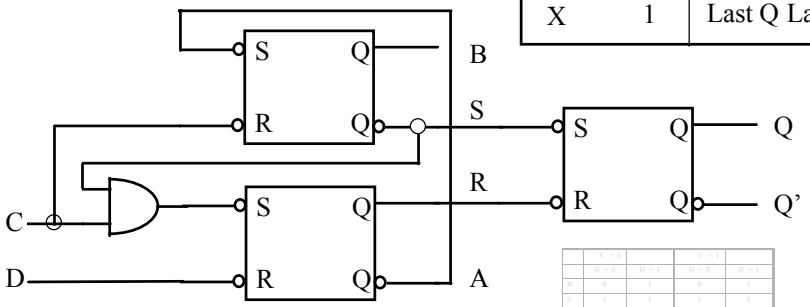
C	D	Q	/Q
1	0	0	1
1	1	1	0
0	X	Last Q	Last /Q

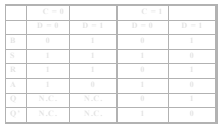
Store a data bit, not set/reset
"Transparent latch"
No illegal operation problem
Setup and Hold time

Positive-Edge-Triggered D Flip-Flop

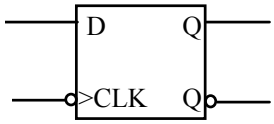


D	CLK	Q	/Q
0	↑	0	1
1	↑	1	0
X	0	Last Q	Last /Q
X	1	Last Q	Last /Q



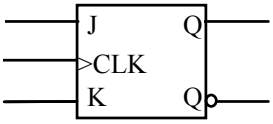


Negative-Edge-Triggered D Flip-Flop

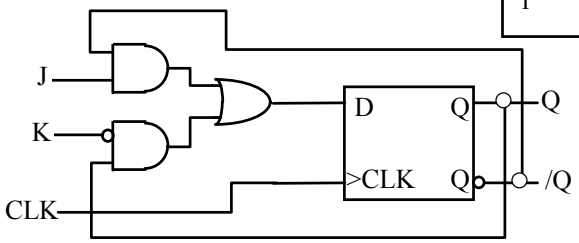


D	CLK	Q	/Q
0	↓	0	1
1	↓	1	0
X	0	Last Q	Last /Q
X	1	Last Q	Last /Q

Edge-Triggered J-K Flip-Flop

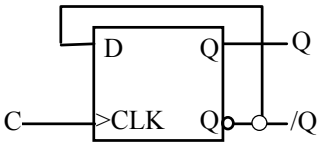


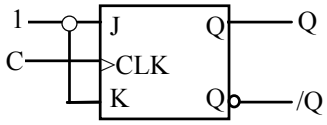
J	K	C	Q	/Q
X	X	0	Last Q	Last /Q
X	X	1	Last Q	Last /Q
0	0	↑	Last Q	Last /Q
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	Last /Q	Last Q



T (toggle) Flip-Flop

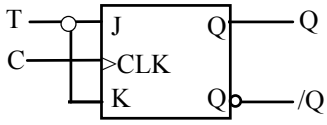
- A T flip-flop changes state on every clock tick.
- Possible circuit designs
  - T without enable





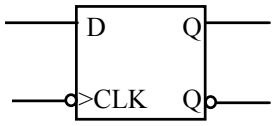
T	CLK	**Q**	**/Q**
0	↑	Q	/Q
1	↑	/Q	Q
X	0	Q	/Q
X	1	Q	/Q

T with enable

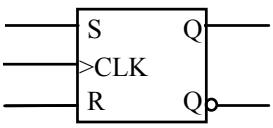


Flip-Flop

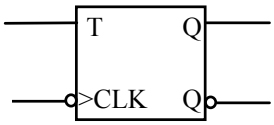
D F.F.



SR F.F.



T F.F.



JK F.F.