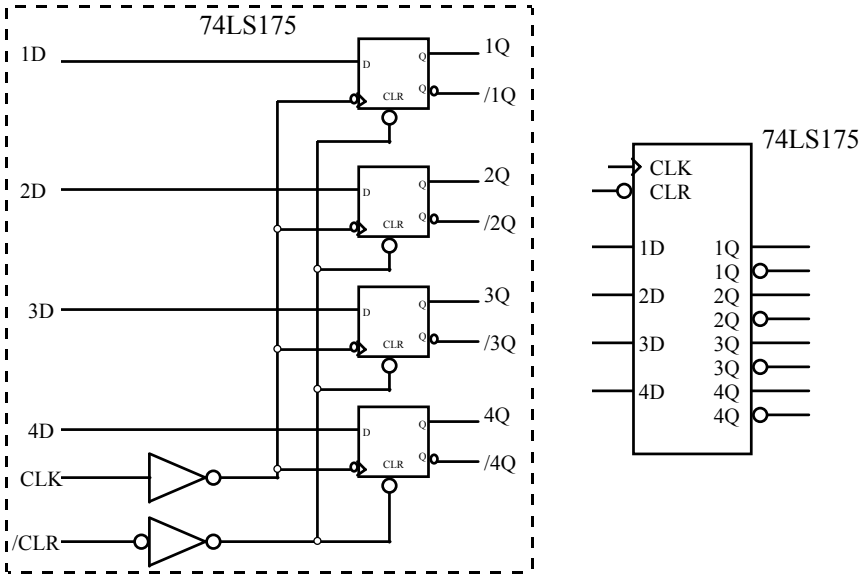
Chapter 3

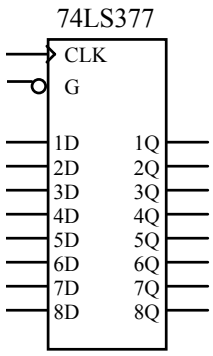
Registers, Counters, Shift Registers

Process Control

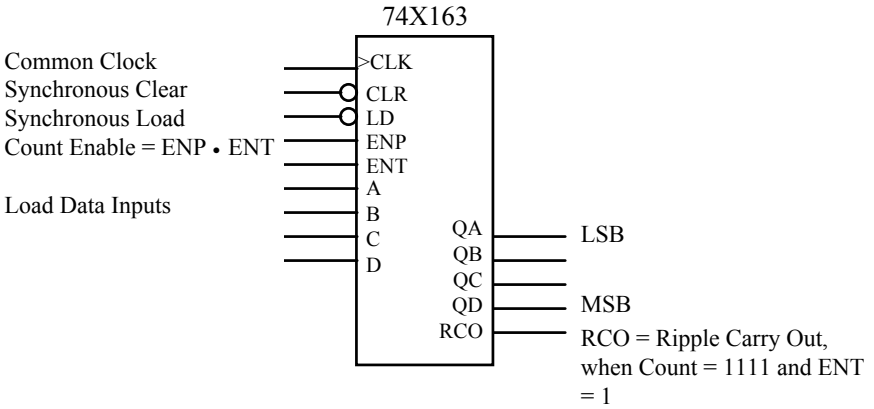
MSI Quad Registers



Octal Register with Clock Enable



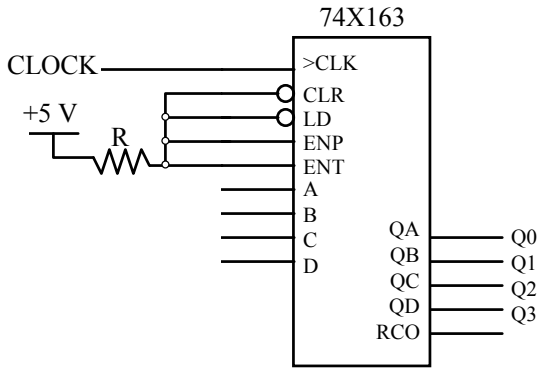
74163 4-bit Synchronous Parallel Counter



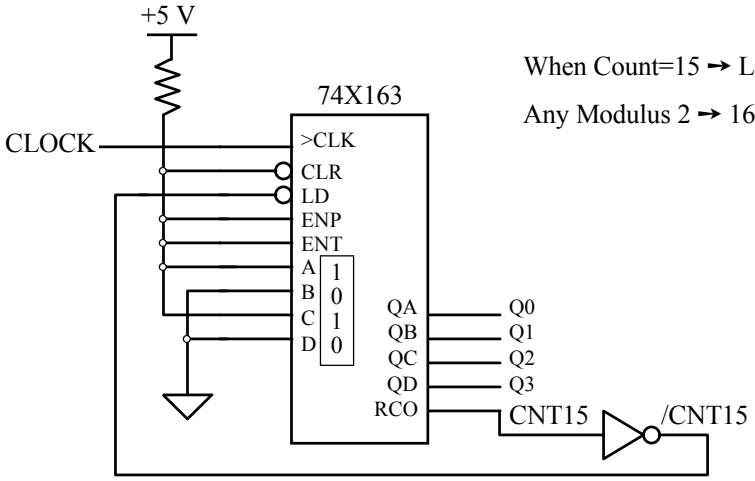
74163 State Table

Inputs					Current State				Next State			
/CLR	/LD	ENT	ENP		Q_D	Q_C	Q_B	Q_A	Q_D*	Q_C*	Q_B*	Q_A*
0	X	X	X	Clear	X	X	X	X	0	0	0	0
1	0	X	X	Load	X	X	X	X	D	C	B	A
1	1	0	X	Hold	X	X	X	X	Q_D	Q_C	Q_B	Q_A
1	1	1	0	Hold	X	X	X	X	Q_D	Q_C	Q_B	Q_A
1	1	1	1	Count	0	0	0	0	0	0	0	1
1	1	1	1	.	0	0	0	1	0	0	1	0
1	1	1	1	.	0	0	1	0	0	0	1	1
1	1	1	1	.	0	0	1	1	0	1	0	0
1	1	1	1		0	1	0	0	0	1	0	1
1	1	1	1		0	1	0	1	0	1	1	0
1	1	1	1		0	1	1	0	0	1	1	1
1	1	1	1		0	1	1	1	1	0	0	0
1	1	1	1		1	0	0	0	1	0	0	1
1	1	1	1		1	0	0	1	1	0	1	0
1	1	1	1		1	0	1	0	1	0	1	1
1	1	1	1		1	0	1	1	1	1	0	0
1	1	1	1		1	1	0	0	1	1	0	1
1	1	1	1		1	1	0	1	1	1	1	0
1	1	1	1		1	1	1	0	1	1	1	1
1	1	1	1		1	1	1	1	0	0	0	0

Application - Free Running Modulo-16 Counter



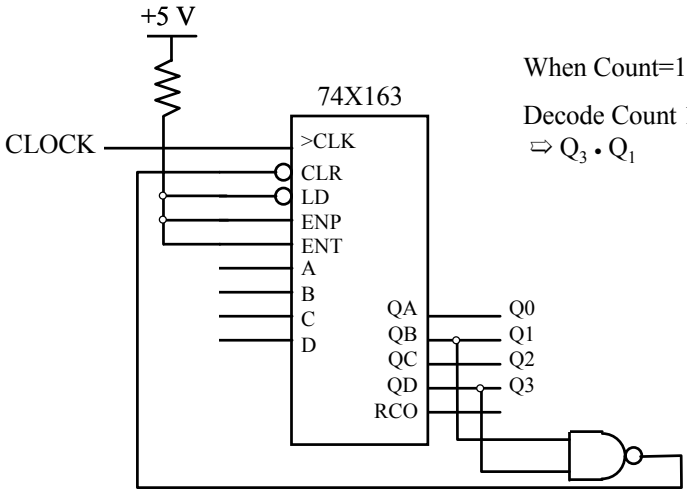
Modulo-11 Counter [5,6, …, 15, 5, 6, ...]



When Count=15 ➙ Load 5 (0101)

Any Modulus 2 ➙ 16 possible

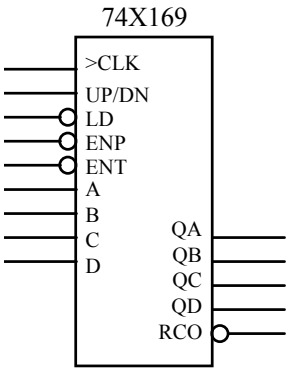
Modulo-11 Counter [0,1,2, …, 10, 0, 1, ...]



When Count=10 ➙ Clear

Decode Count 1x1x (10…15)
⇨ $Q_3 \cdot Q_1$

74169 Up/Down Counter

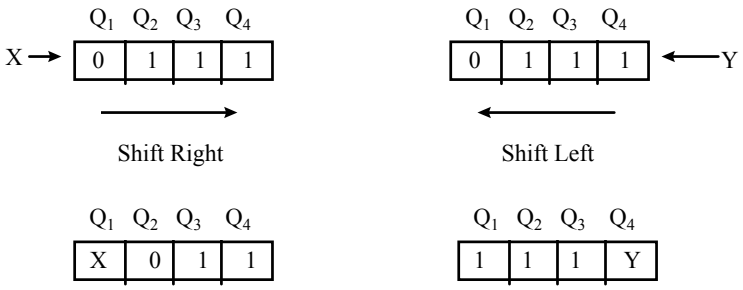


UP/DN = 1 = up → RCO = 15
UP/DN = 0 = down → RCO = 0

up down up
Ex: 0,1,2, 1,0,15,14, 15,0,1,2
RCO RCO

Shift Registers

- Multi-bit register that moves data “sideways” left/right (1 bit/clock)

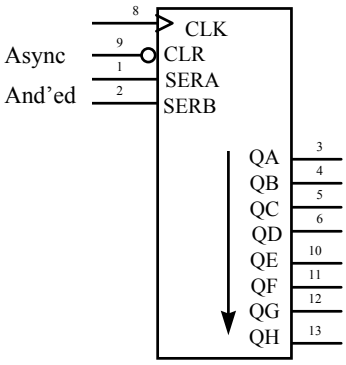


⇨ Often used to rearrange bits or Multiply/Divide by 2

MSI Shift Registers

Octal (8-bit) SIPO

74X164



Octal (8-bit) SISO, PISO

74X166