Use The PC's Parallel Port For Fast Data Acquisition And Control

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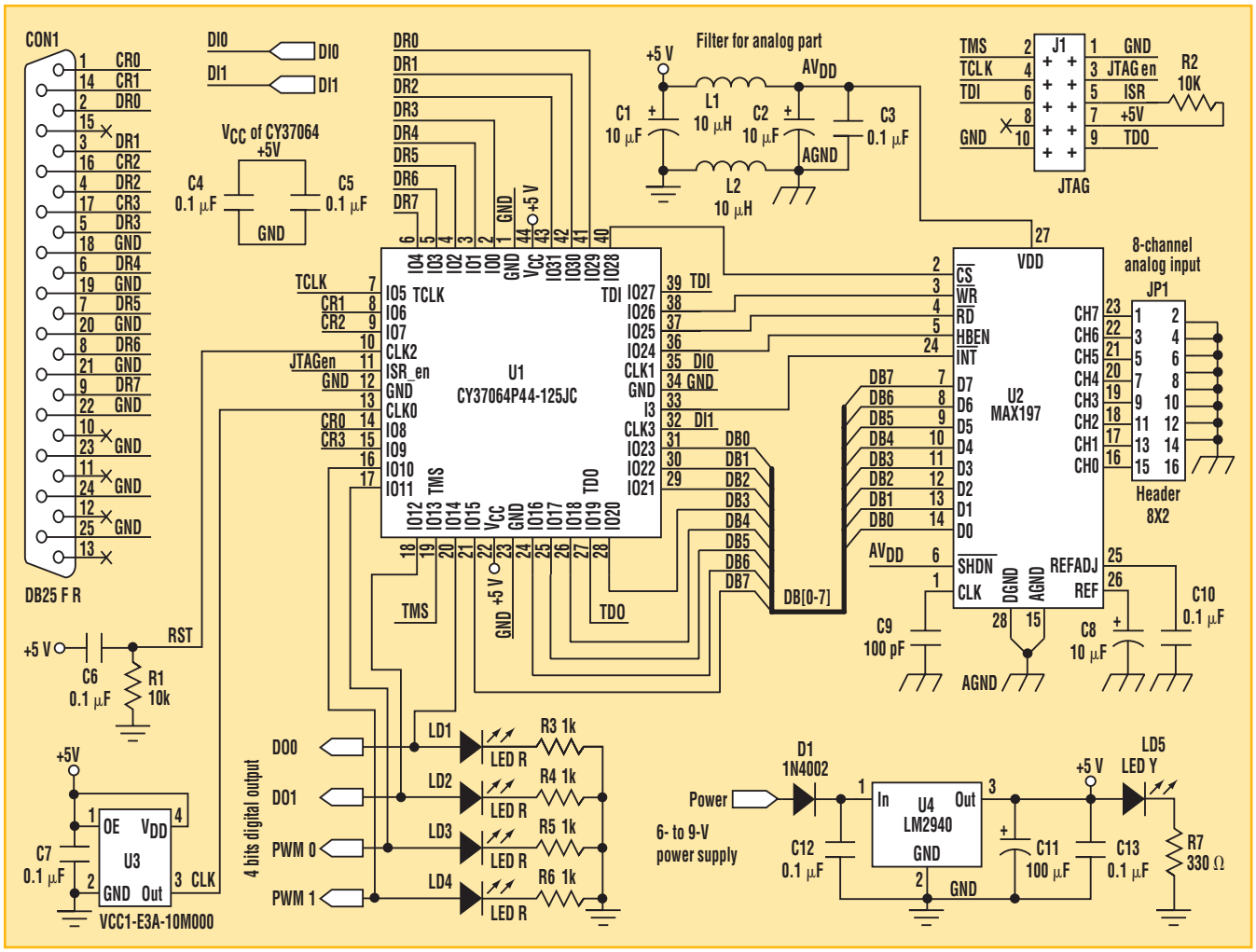
Many designers require that their PCs act as complete control systems without any internal hardware. For this function, users need at least one channel of analog data acquisition to monitor the controlled signal. They also require one digital output channel to handle the external element's on/off function.

For precise control, users must replace the on/off control with proportional, integral, derivative (PID) control, which means replacing the Digital Out signal with Analog Out or pulse-width modulation (PWM). Some applications will need more than one channel.

When implemented, the control circuit includes eight channels of 12-bit analog-to-digital (a-d) conversion, two bits of Digital Out (DO), two bits of PWM, and two bits of Digital In (DI). They're all connected to the PC through the parallel port in Enhance Parallel Port (EPP) mode *(see the figure)*. In EPP



With this CPLD-based circuit, designers can use the PC as a complete control system. It includes eight channels of 12-bit a-d conversion, two bits of DO, two bits of PWM, and two bits of DI, all connected to the PC through the parallel port.

mode, the port is an 8-bit bidirectional bus with four control bits. A complete I/O cycle takes around 1 µs, so the maximum transfer rate is about 1 Mbyte/s. Because the a-d conversion takes several I/O cycles, the analog transfer rate is about 100 kHz. Moreover, the switching between input and output mode is very fast—1 µs—so the system has quick response times.

Modern digital designs are increasingly based on CPLDs. Flexible and inexpensive, the CPLDs replace many "old-fashioned" logic parts with a single high-density device. Designs can be very compact, small in size, and ultra fast. There are several methods to design, synthesize, and simulate the contents of the CPLD: hardware description languages such as Verilog, VHDL, and schematic editors. WARP 6.0 VHDL from Cypress Semiconductor was used to synthesize and simulate the CPLD in the figure.

The most significant device in this circuit is U1, the Cypress Semiconductor CY37064P44 CPLD with 64 macro cells and 44 pins. It implements all of the circuit's logic in a chip set. Because the parallel port doesn't include an address bus, the system must read or write any data with two cycles: first writing the address, then reading or writing the relevant data. Using this architecture, each register in the chip set has its own address:

0-ADCL: Read low byte of ADC.
1-ADCH: Read high byte of ADC.
2-ADCS: Write start conversion/Read end of conversion.
3-Digital: Write 2 DO bits/Read 2 DI bits.
4-PWM: Write 8 bits duty cycle for PWM.
5-PWMen: Write 2 bits to Enable/Disable PWM output.

The circuit's second device, U2, is Maxim's MAX1973 multirange, 12-bit data-acquisition system. It requires only a single +5-V supply. The circuit provides eight analog input channels that are independently software programmable for a variety of ranges: ±10 V, ±5 V, 0 to +10 V, or 0 to +5 V. This setup gives users the flexibility to interface with industrial sensors (4-20 mA, ±12 V, and ±15 V). In addition, the converter has an overvoltage protection of up to ±16.5 V and can work at a rate of 100 ksamples/s.

U2 is configured to use an internal clock and an internal reference by connecting C8, C9, and C10 to the analog ground. Conversions are initiated with a writing of a control byte to ADCS. The format of a control byte is: "0-1-0-R-B-A2-A1-A0," where R is a range (0 = 5 V, 1 = 10 V), B is a polarity (0 = unipolar, 1 = bipolar), and A2-A1-A0 is the channel index in binary code.

For example, to operate channel 3 with a range of 10 V, the user must write "01011011" to ADCS. As noted before, the user needs only to send a byte to the parallel port. All other signals (DB, CS, WR, RD, and so on) are controlled by the CPLD. After the conversion is complete, U2 is signaled by the INT pin, which can be read through bit 0 of ADCS. Then, the user can read the low byte (ADCL) and the high byte (ADCH) of the result.

To write or read the digital bits, the user must write or read the relevant data to or from the two LSBs of digital (address 3). To set the duty cycle of the PWM output between 0° and 360°, users should write an 8-bit binary number to the PWM register (address 4). Enabling or disabling the PWM output is accomplished by setting or clearing the two LSBs of the PWMen register (address 5).

U3 is 10-MHz clock. The five components—C1, C2, C3, L1, and L2—are filters for the power pins of the analog part. R1 and C6 are power-on reset. All LEDS are low current (2 mA). U4 is a low-drop +5-V regulator.

From the programmer's point of view, there's a need for three low-level functions: writeAddress, writeData, and readData. Those functions can be written in assembly, C, or any other high-level language *(see Listing 1 under the Ideas for Design heading at* www.elecdesign.com).

Designers may program the CPLD with any industrial parallel CPLD programmer, but the best method is to use the in-system reprogramming (ISR) feature. J1 is a JTAG port designed for this purpose. Users simply connect the UltraISR or C3ISR programming cable between J1 and the PC, load the JEDEC file, and program the device *(see Listing 2 at* www.elecdesign.com). Readers can use the JEDEC file to program the CPLD or synthesize the VHDL source file. Moreover, readers can modify the VHDL source file for their own applications *(see Listing 3 at* www.elecdesign.com).