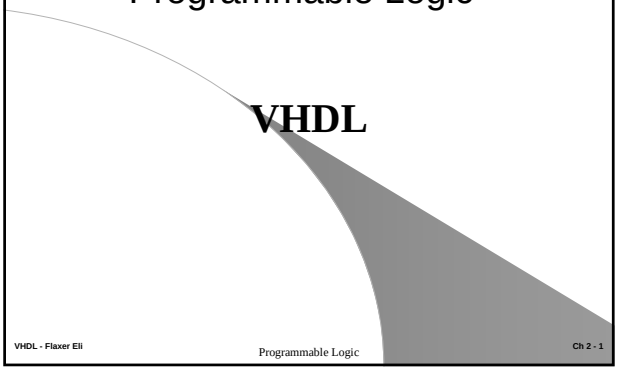
Chapter 2
Programmable Logic



Review (last chapter)

- VHDL and programmable logic = best current solution for rapid design, implementation, testing, and documenting of complex digital systems.
- Standard 6-step design synthesis process
- General flow of information through standard VHDL synthesis CAD tools
- Features of the three VHDL CAD tools available (Warp2, Max+Plus2, and Workview)
- VHDL code example and three architectural styles of VHDL

Course Objectives Affected

- Write VHDL code that can be implemented efficiently in a given technology device.
- Describe and select the appropriate PLDs, CPLDs, and FPGAs from several popular vendors (e.g. Altera, Cypress, and Xilinx) that satisfy system requirements.

Outline

- What is programmable logic?
- Why use programmable logic?
- How it is programmed
- How to compare devices
- Cypress device details

Programmable Logic Definitions

- Digital integrated circuit
  - whose logic functions are determined by the application design engineer
  - and implemented locally
- Many types of programmable logic
  - sometimes generically called PLDs (Programmable Logic Devices)
  - PAL
  - PLD
  - CPLD
  - FPGA

Programmable Logic Definitions

- PAL (Programmable Array Logic)
  - simple programmable And/Or array
- PLD (Programmable Logic Device)
  - programmable And/Or array
  - include input/output flip-flops
- CPLD (Complex Programmable Logic Device)
  - array of multiple PLD-like blocks
  - programmable interconnects between blocks
- FPGA (Field Programmable Gate Array)
  - array of simple logic cells
  - interconnected via wires within routing channels

Advantages of Programmable Logic

- Design flexibility
- Better design automation
- Higher density, fewer packages
- Less expensive
- Lower power
- Higher performance

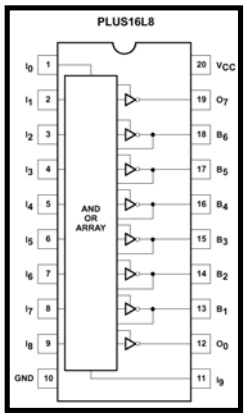
Programming Technologies

- Interconnections usually made by pass transistors controlled by memory bits of some type:
- EPROM - charged floating gate, UV erasable
- EEPROM - charged floating gate, electrically erasable
- Flash Memory - charged floating gate, electrically erasable
- SRAM - Volatile memory
- Antifuse - permanent connections made electrically

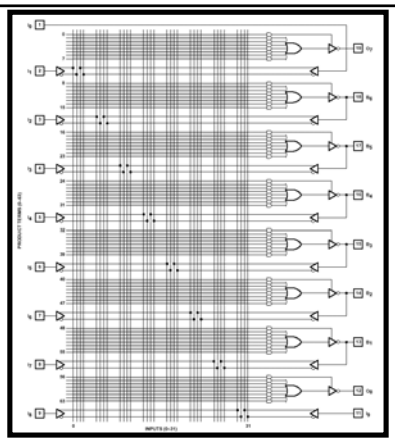
Device Databook Examples

- PAL - GAL 16L8
- PLD - PALCE 22V10
- CPLD - CY37000
- GPLD - Delta39K
- FPGA - FLEX 10K

PAL 16L8

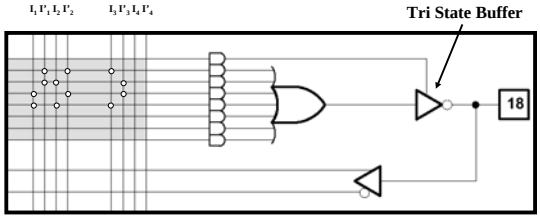


PAL 16L8



Function Implementation by PAL

$$F = I_1 \oplus I_2 \oplus I_3 = I'_1 I'_2 I_3 + I'_1 I_2 I'_3 + I_1 I'_2 I'_3 + I_1 I_2 I_3$$



VHDL Example

```
--   Example VHDL code for 3-bit XOR
LIBRARY ieee;
USE ieee.std_logic_1164.all;
              ------------------------------------------------------
ENTITY My3xor IS
  PORT (a,b,c: IN std_logic;        --inputs
                y:    OUT std_logic);              --output
 END My3xor;
 ------------------------------------------------------
ARCHITECTURE DataFlow OF My3xor IS
BEGIN
              y <= ((a xor b) xor c);
END DataFlow;
```


Equations Result

```
--------------------------------------------------------------------------------
PLD Compiler Software:       PLA2JED.EXE    31/03/2000  [v4.02 ] 6.2
IR 27

DESIGN EQUATIONS          (02:04:56)


   y =
        a * b * c
      + /a * /b * c
      + /a * b * /c
      + a * /b * /c


Completed Successfully
--------------------------------------------------------------------------------
```


PinOut Result

```
PINOUT INFORMATION    (02:04:56)

Messages:
 Information: Checking for duplicate NODE logic.
              None.

                        C16V8A
                  ____________________________________
              c =| 1|                        |20|* not used
              b =| 2|                        |19|= y
              a =| 3|                         |18|* not used
     not used *| 4|                         |17|* not used
     not used *| 5|                         |16|* not used
     not used *| 6|                         |15|* not used
     not used *| 7|                         |14|* not used
     not used *| 8|                         |13|* not used
     not used *| 9|                         |12|* not used
     not used *|10|                         |11|* not used
                  ____________________________________
Summary:
              Error Count = 0      Warning Count = 0

Completed Successfully
--------------------------------------------------------------------------------
```

Utilization Result

RESOURCE UTILIZATION (02:04:56)

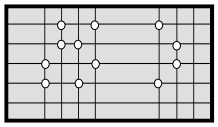
Information: Output Logic Product Term Utilization.

Node#	Output Signal Name	Used	Max
12	Unused	0	7
13	Unused	0	7
14	Unused	0	7
15	Unused	0	7
16	Unused	0	7
17	Unused	0	7
18	Unused	0	7
19	y	4	7

4 / 56 = 7 %

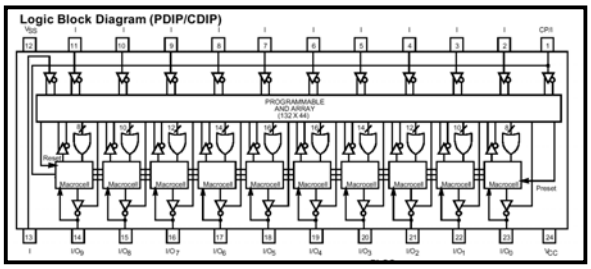
Completed Successfully

JEDEC File



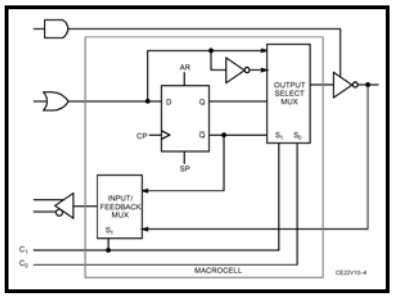
```
NOTE DEVICE C16V8A*
NOTE PACKAGE palce16v8-7jc*
NOTE PROPERTY BUS_HOLD ENABLE*
NOTE PINS  c:1 b:2 a:3 y:19 *
NOTE PINS *
L00000
11111111111111111111111111111111
10100111111111111111111111111111
10011011111111111111111111111111
01101011111111111111111111111111
01010111111111111111111111111111
00000000000000000000000000000000
00000000000000000000000000000000
00000000000000000000000000000000
* Node y[19] => OE : 1 ,LOGIC : 7 *
```


PALCE 22V10 Block Diagram



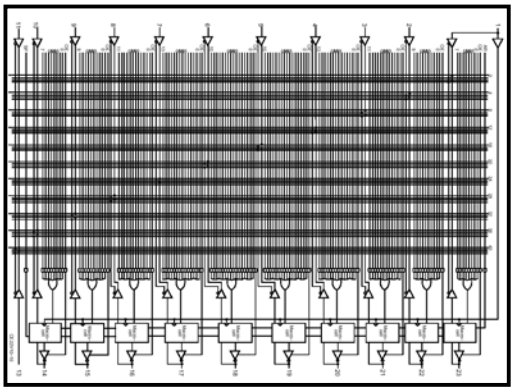
- Max 22 inputs
- Max 10 outputs
- 1 Clock (pin 1 CP)

PALCE 22V10 Macro Cell

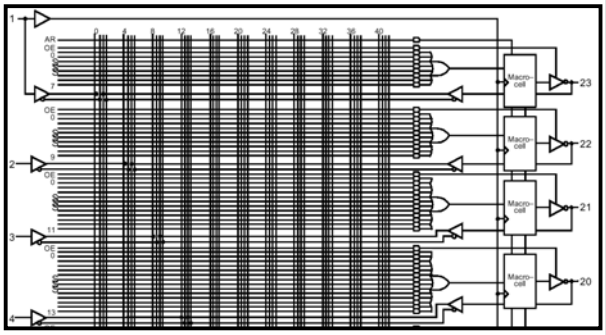


Asynchronous Reset (AR)
Synchronous Preset (SP)
Common Clock (CP)

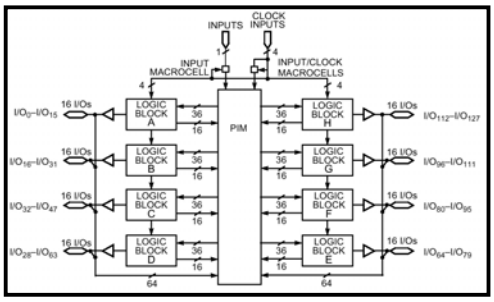
PALCE 22V10 Connections



PALCE 22V10 Matrix

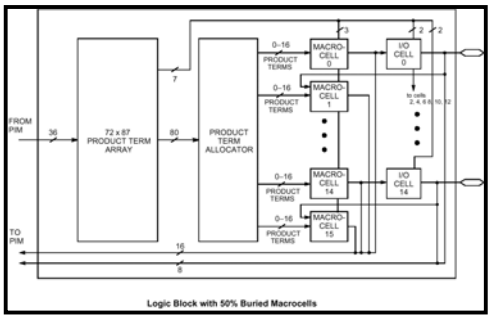


Ultra 37000 Block Diagram



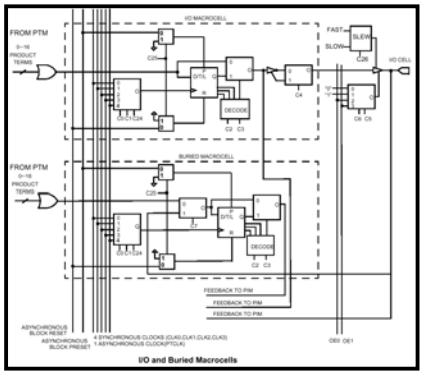
- Logic Block is similar to PLD
- 4 Clock

Ultra 37000 Logic Block



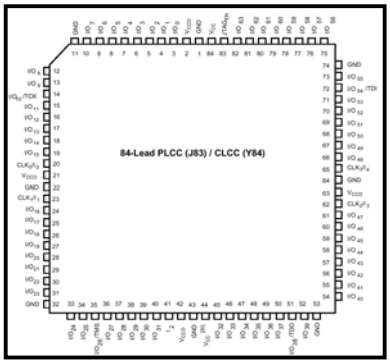
- PIM - Product Interconnection Matrix

Ultra 37000 Macro-Cell

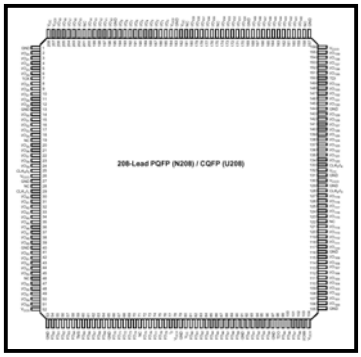


- Async Reset
- Astnc Preset
- 4 Clock Input
- Tri-State I/O
- 1 Async Clock

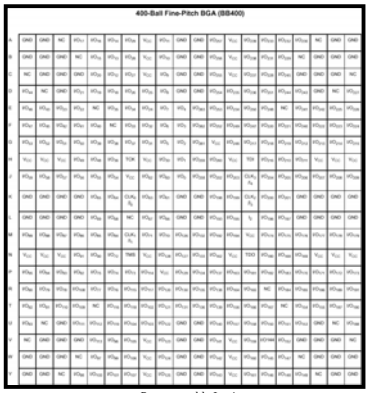
Ultra 37128 PLCC 84



Ultra 37256 PQFP 208



Ultra 37512 BGA 400



Ultra 37000 Information & Device Package

General Information

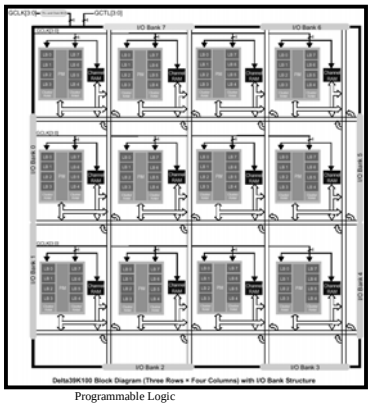
Device	Macrocells	Dedicated Inputs	I/O Pins	Speed (t_{PD})	Speed (f_{MAX})
CY37032	32	5	32	6	200
CY37064	64	5	32/64	6	200
CY37128	128	5	64/128	6.5	167
CY37192	192	5	120	7.5	154
CY37256	256	5	128/160/192	7.5	154
CY37384	384	5	160/192	10	118
CY37512	512	5	160/192/264	10	118

Device-Package Offering & I/O Count

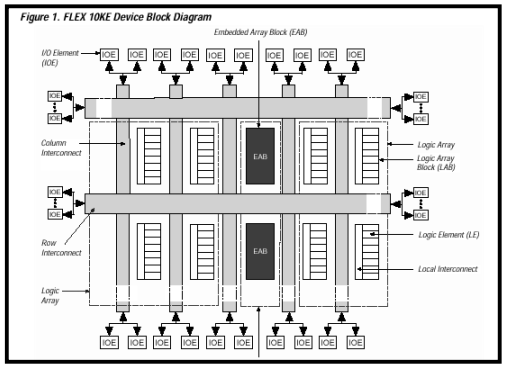
Device	44-Lead TQFP	44-Lead PLCC	44-Lead CLCC	84-Lead PLCC	84-Lead CLCC	100-Lead TQFP	160-Lead TQFP	160-Lead CQFP	208-Lead PQFP	208-Lead CQFP	256-Lead BGA	352-Lead BGA
CY37032	37	37										
CY37064	37	37	37	69		69						
CY37128				69	69	69	133					
CY37192							125					
CY37256							133	133	165		197	
CY37384									165		197	
CY37512									165	165	197	269

Delta 39K Block Diagram

- Logic Unit is similar to CPLD
- RAM



FLEX 10K Block Diagram



Summary

- Defined Programmable Logic, PAL, PLD, CPLD, GPLD, FPGA, and their characteristics
- Advantages of Programmable Logic - Design flexibility, Better design automation, Higher density, fewer packages, Less expensive, Lower power, Higher performance
- Programming Technologies - EPROM, EEPROM, Flash memory, SRAM, Antifuse
- Details of Cypress programmable logic - PALCE22V10, CY37000, Delta39K and Altera FLEX10K.